

Remarks

Claims 1-6, 9-16, 18-20, 22-24, and 26-28 were presented in the previous amendment. The Examiner has rejected claims 1-6, 9-16, 18-20, 22-24, and 26-28. By this amendment, claims 1 and 15 are amended. Thus, claims 1-6, 9-16, 18-20, 22-24, and 26-28 remain in this application.

The Examiner rejected claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 under 35 USC §102(b) as being anticipated by Nemirovsky (DISC, A Dynamic Stream Computer). More specifically, the examiner stated that Nemirovsky taught the invention as claimed including a processor executing a plurality of streams (page 63), a set of functional resources (page 101 and 102), interrupt logic (page 96) and interrupts directed to one or more specific streams (page 63).

With respect to claim 1, it is repeated below for ease of reference:

1. (currently amended) A multi-streaming processor comprising:
 - a plurality of hardware streams for streaming one or more instruction threads;
 - a set of functional resources coupled to said hardware streams for processing instructions from said streams;
 - interstream control coupled to said functional resources including a master mode wherein more than one stream is accorded master status, and the streams accorded master status may each run a master thread exercising master control over other streams not under control of another master stream;
 - interrupt detection logic, coupled to interrupt signals, for providing said interrupt signals to the processor;
 - interrupt mapping logic, for providing configurable interrupt mapping of said interrupt signals to ones of said plurality of streams such that at least one of said interrupt signals is mapped to ones of said plurality of streams; and
 - interrupt logic, coupled to said interrupt mapping logic, for interrupting one or more of said streams according to said configurable interrupt mapping provided by said interrupt mapping logic;

wherein through said interrupt logic, said interrupts are detected, and at the time of their detection said ones of said plurality of streams are directed to process said interrupts.

Applicant respectfully suggests that his reading of Nemirovsky is a bit different. Applicant agrees with the examiner in that Nemirovsky discloses a processor executing a plurality of streams, and interrupt logic. However, Applicant does not believe that the interrupt logic is directed at one *or more* specific streams. Rather, Nemirovsky states that “Every IS (instruction stream) has *one* interrupt register (IR) and *one* mask register (MR). On DISC1 the interrupt registers contain 8 bits, bit 7 is the highest priority, bit 0 is the lowest priority (or background or normal mode of running). Interrupt 7 to 1 are vectored interrupts.... [sic] When no bit of the IS is set, the instruction stream will not be scheduled (not active). Once an interrupt is requested, if it is the highest priority one pending, a vector interrupt will be generated. The next instruction that belongs to *that* IS will be started at the address given by the vector interrupt.” at page 167 of Applicant’s copy of Nemirovsky, [emphasis added]. Applicant understands this to mean that Nemirovsky teaches the use of an interrupt register for each instruction stream, which defines the priority of interrupts for that instruction stream. Applicant has reviewed Nemirovsky and has not found any teaching of the use of interrupt mapping logic to allow mapping of an interrupt to one or more instruction streams. Applicant stated such in the previously submitted Amendment E. The examiner failed to respond to Applicant’s arguments. Rather, the Examiner simply repeated his previous argument and rejected claim 1, as a Final Rejection. Applicant respectfully requests that the Examiner indicate where in Nemirovsky (DISC, A Dynamic Stream Computer), an interrupt signal can be mapped to more than one instruction stream.

Claim 1, as amended, particularly recites “interrupt mapping logic, for providing configurable interrupt mapping of said interrupt signals to ones of said plurality of streams”. Applicant respectfully suggests that such mapping of interrupt signals to one or more streams is nowhere taught, suggested, or even hinted at by Nemirovsky. Nowhere can applicant find a teaching in Nemirovsky which maps an interrupt to more than one instruction stream. In fact, applicant has converted a .pdf of Nemirovsky into an electronically searchable format, and searched for every instance of the term interrupt.

The result of this search confirms Applicant's statement that nowhere does Nemirovsky teach the mapping of an interrupt to more than one interrupt. In fact, Nemirovsky teaches just the opposite. In Applicant's copy, page 164, 2d column, lines 13-17, Nemirovsky states "It is thus possible to assign an interrupt to *a given stream* which begins processing effectively in parallel and at *a given level* of partitioned throughput ... (emphasis added). Nemirovsky continues to show an advantage of actually not allowing that interrupt to impact the throughput of the other instruction streams by that interrupt! Further, on page 169, column 1, lines 45-48 Nemirovsky states "By *dedicating a stream to a particular interrupt*, we can achieve very high figures of merit... (emphasis added)" Thus, from Applicant's reading of Nemirovsky, every use of the term interrupt implies that an interrupt is dedicated to a particular instruction stream, not mapped to one or more instruction streams.

Further, nothing in Nemirovsky is directed at utilization of such mapping logic to, upon interrupt detection, to direct one or more streams to process the interrupts. And, claim 1 particularly recites interstream control coupled to the set of functional resources, where more than one stream can be accorded master status exercising master control over other streams not under control of another master stream. For these reasons, Applicant respectfully suggests that claim 1, as amended, is novel and non-obvious over Nemirovsky. Applicant requests the Examiner to withdraw his rejection of this claim as amended.

As to claims 2-3, 5-6, and 9-12, these depend either directly or indirectly from claim 1 and add further limitations that are neither anticipated nor obviated by Nemirovsky. For the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 15, it is repeated below as amended for ease of reference:

15. (currently amended) A method for processing an interrupt in a multi-stream processor having a plurality of hardware streams, comprising:

implementing interstream control in the processor wherein a stream may exert control functions on one or more of the plurality of hardware streams;

establishing control access privileges associated with each of the plurality of hardware streams;

exercising interstream control between the plurality of hardware streams, the interstream control utilizing said step of establishing control access privileges to assure compliance of controlled streams;

detecting the interrupt and passing the detected interrupt to interrupt mapping logic;

determining, using the interrupt mapping logic, which ones of the plurality of hardware streams are to be interrupted by the interrupt; and

interrupting the ones of the plurality of hardware streams that are to be interrupted by the interrupt.

Claim 15 specifically recites a method for processing an interrupt in a multi stream processor where interrupt mapping logic determines which ones of a plurality of hardware streams are to be interrupted by the interrupt. As mentioned above with respect to claim 1, applicant cannot find any teaching in Nemirovsky where an interrupt is mapped to more than one instruction stream. For this reason, and for those stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 16, 18-20, 22-24, 26-28, these depend either directly or indirectly from claim 15 and add further limitations that are neither anticipated nor obviated by Nemirovsky. For all of the reasons stated above with respect to claims 1, 2 and 15, applicant respectfully requests the examiner to withdraw his rejection of these claims.

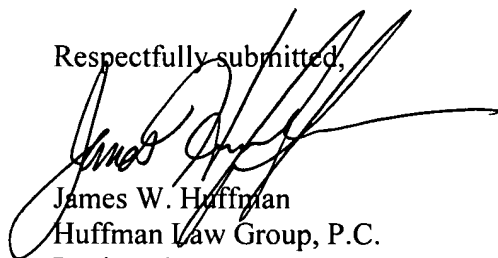
Applicant has reviewed the file history of office actions and amendments to date and wishes to respond to one further note by the examiner. More specifically, the examiner stated that "applicant's admission on paper no. 8, last paragraph of page 8 continued on to page 9, set forth that conditional and dynamic mapping is well-known in the art." Applicant wishes to make clear that mapping of an interrupt to an instruction stream was taught by Nemirovsky. However, what was not taught by Nemirovsky, or admitted in the file history, is the novel feature of the present invention, which is the mapping, whether

static or dynamic, of an interrupt to one or more hardware streams within a multi-streaming processor. Applicant pointed this out in his Amendment E, to which no comment was provided by the Examiner.

For all of the above reasons, applicant respectfully requests the examiner to withdraw his rejection of all of the remaining claims, and that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,



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